ABSTRACT OF THE DISCLOSURE

An architecture for a pipeline processor circuit, preferably of the VLIW type, comprises a plurality of stages and a network of forwarding paths which connect pairs of said stages, as well as a register file for operand write-back. An optimization-of-power-consumption function is provided via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network on account of their reduced liveness length.